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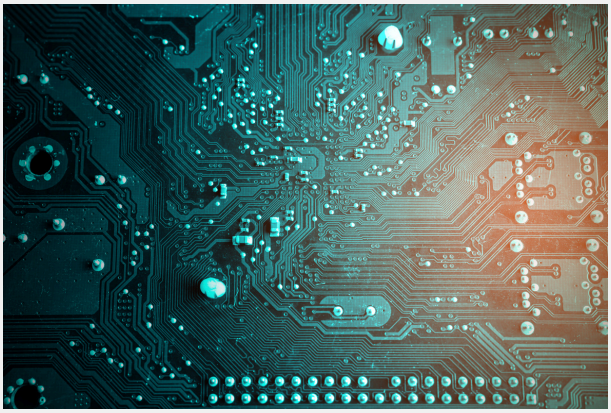
# SVx

# GenAI Automated Security-Aware Formal Assertion Generation



## What is SVx?

SVx is a GenAI based security solution for automated security-aware formal property generation. It surpasses security static checks by identifying deeper threats and incorporating threat modeling for proactive detection of vulnerabilities.

SVx analyzes the RTL design and its specification with user-selected threat modeling to identify critical security assets. It then creates natural language security properties that define the design's expected security behavior, which are subsequently converted into SystemVerilog assertions which are compatible with any industry standard formal verification tool.

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# What are the benefits of SVx?

- **Threat models driven approach:** SVx uses structured threat models to guide security validation, ensuring checks are aligned with real-world attack scenarios.
- **Early detection of security weakness:** By integrating into early design stages, SVx identifies vulnerabilities before they propagate, reducing downstream security risks and costly rework.
- **Fast and accurate formal assertion generation:** SVx automates the creation of precise formal security processes, speeding up verification while reducing human error.
- **Compatible across Verilog and SystemVerilog:** SVx works seamlessly with both Verilog and SystemVerilog designs, making it versatile for a wide range of hardware development flows.
- **Design privacy ensured - security through localized LLMs:** SVx uses localized large language models, meaning your proprietary design data stays secure and private - never leaving your environment.
- **Ensuring confidence levels through security coverage metrics:** SVx quantifies verification progress with security-specific coverage metrics, helping teams assess how thoroughly security threats are addressed.